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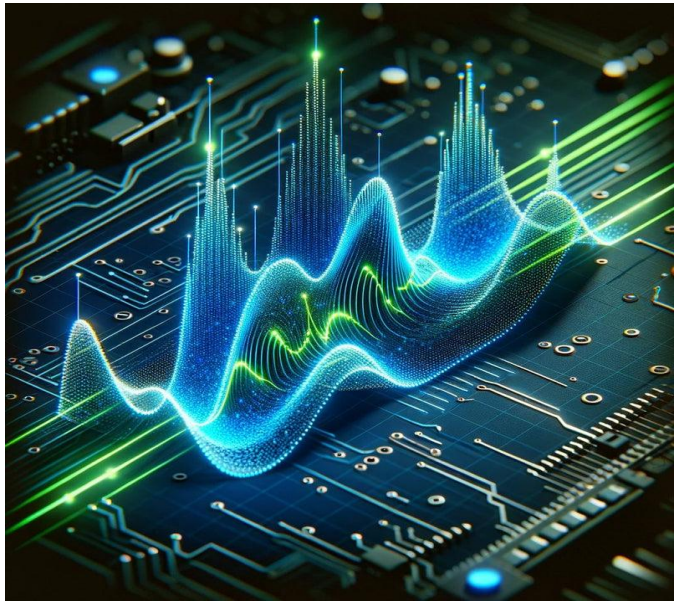
22EE603 – PRINCIPLES OF DIGITAL SIGNAL PROCESSING



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22EE603 – PRINCIPLES OF DIGITAL SIGNAL PROCESSING - CO's

CO1	Illustrate the basics of discrete time signals and systems. [U]
CO2	Interpret the concepts of Discrete and Fast Fourier transform [U]
CO3	Comprehend the architecture of advanced processors. [U]
CO4	Apply the concept of transformation techniques in Discrete Time systems. [AP]
CO5	Design different types of filters using various filter design techniques. [AP]

22EE603 – PRINCIPLES OF DIGITAL SIGNAL PROCESSING - Modules

1	Signals and Systems
2	Discrete Fourier Transform and Fast Fourier Transform
3	FIR Filters, IIR Filters and Digital Signal Processors

MODULE – III : FIR Filters, IIR Filters and Digital Signal Processors

3.1	Design of FIR filters
3.2	Design of IIR filters
3.3	Architecture of TMS320C64xx processor

3.3 Architecture of TMS320C64xx processor

Introduction:

- A digital signal processor is a specialised microprocessor targeted at digital signal processing applications.
- Digital signal processing applications demand specific features that paved the way for Programmable Digital Signal Processors (P-DSP).
- Unlike the conventional microprocessors meant for general-purpose applications, the advanced microprocessors such as Reduced Instruction Set Computer (RISC) processors and Complex Instruction Set Computer (CISC) processors may use some of the techniques adopted in P-DSP, or may even have instructions that are specifically required for DSP applications.

3.3 Architecture of TMS320C64xx processor

The salient features required for efficient performance of DSP operations are:

(i) Multiplier and Multiplier Accumulator

(ii) Modified Bus Structure and Memory Access Schemes

(iii) Multiple Access Memory

(iv) Multiported Memory

(v) Very Long Instruction Word (VLIW) Architecture

(vi) Pipelining

(vii) Special Addressing Modes

(viii) On-Chip Peripherals

3.3 Architecture of TMS320C64xx processor

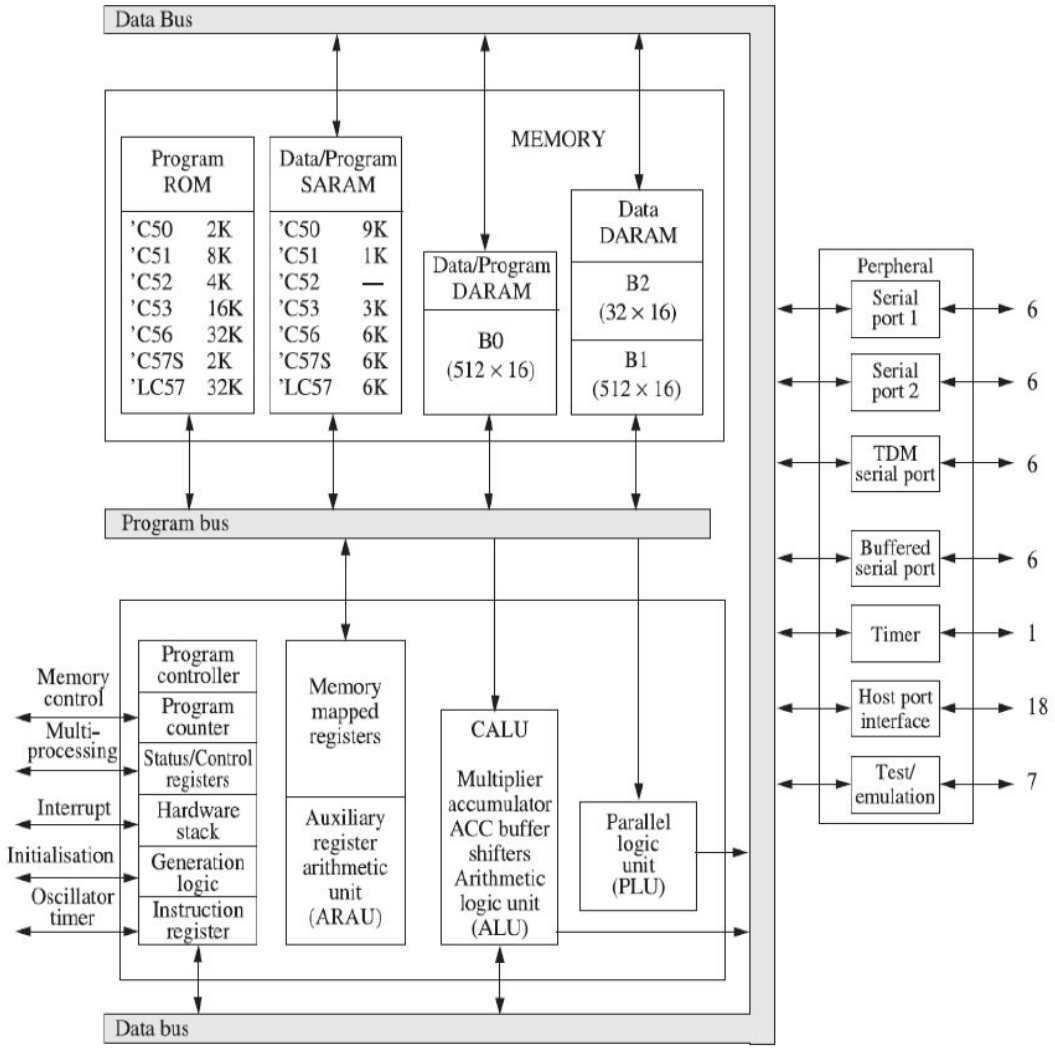
Advantages of DSP Processors:

- DSP processors are often tuned to meet the needs of specific digital signal processing applications.
- DSP processors strong in terms of performance.
- The development time can be reduced significantly with proper use of high level programming modules.
- A DSP processor offers shorter time to market due it its software programmability.

3.3 Architecture of TMS320C64xx processor

- The TMS320C5X generation of the Texas instruments TMS320C50 digital signal processor is fabricated with CMOS IC technology. It is a fixed point, 16-bit processor running at 40 MHz.
- The single instruction execution time is 50 nsec.
- Its architectural design is based on the combination of advanced Harvard architecture, on-chip peripherals and on-chip memory.
- The TMS320C50 has a programmable memory map which can vary for each application.
- On-chip memory includes 10K words of the RAM and 2K words of the ROM.

3.3 Architecture of TMS320C64xx processor



3.3 Architecture of TMS320C64xx processor

- All C5X DSPs have the same CPU structure. However, they have different on-chip memory configuration and on-chip peripherals.
- The functional block diagram of TMS320CX is shown in Figure. It can be divided into four sub blocks. They are:

(1) Bus structure

(2) Central processing unit

(3) On-chip memory

(4) On-chip peripherals.

3.3 Architecture of TMS320C64xx processor

(1) Bus structure

- Separate program and data buses in the advance Harvard architecture of C5X maximize the processing power and provide a high degree of parallelism.
- Many DSP applications are accomplished using single cycle multiply/accumulate instruction with a data move option.
- The C5X included the control mechanism to manage interrupts, repeated operations and function calling.

3.3 Architecture of TMS320C64xx processor

- The ‘C5X’ architecture has four buses:
  1. Program bus (PB)
  2. Program read bus (PRB)
  3. Data read bus (DB)
  4. Data read address bus (DRB)
- The program bus carries the instruction code and immediate operands from program memory to the CPU.
- The program address bus provides address to program memory space for both read and write.

3.3 Architecture of TMS320C64xx processor

(2) Central processing unit

The CPU consists of the following elements:

1. Central arithmetic logic unit (CALU)
2. Parallel logic unit (PLU)
3. Auxiliary register arithmetic unit (ARAU)
4. Memory mapped registers
5. Program controller

3.3 Architecture of TMS320C64xx processor

3. On-Chip Memory

- The C5X structure has a total memory address range of 224K words _ 16 bits. The memory space is divided into four memory segments.

  - 64K word program memory space: It contains the instruction to be executed.
  - 64K word local data memory space: It stores data used by the instruction.
  - 64K word input/output ports: It interfaces to external memory mapped peripherals.
  - 32K word global data memory space: It can share data with other peripherals within the system.

3.3 Architecture of TMS320C64xx processor

- The large on-chip memory of C5X includes:
  1. Program read only memory
  2. Data/Program single access RAM (SARAM)
  3. Data/Program dual access RAM (DARAM)

4. On-Chip peripherals

- All C5X DSPs have the same CPU structure; however, they have different on-chip peripherals connected to their CPUs. A TMS320C50 digital signal processor contains the following on-chip peripherals.
  1. Clock generator
  2. Hardware timer

3.3 Architecture of TMS320C64xx processor

3. Software programmable wait stage generators

4. General purpose I/O pins

5. Parallel I/O ports

6. Serial port interface

7. Buffered serial port

8. TDM serial port

9. Host port interface

10. User-maskable interrupts

3.3 Architecture of TMS320C64xx processor

DSP Memory Architecture:

DSP processors use special memory architectures, namely, Harvard architecture or modified VonNeumann architecture.

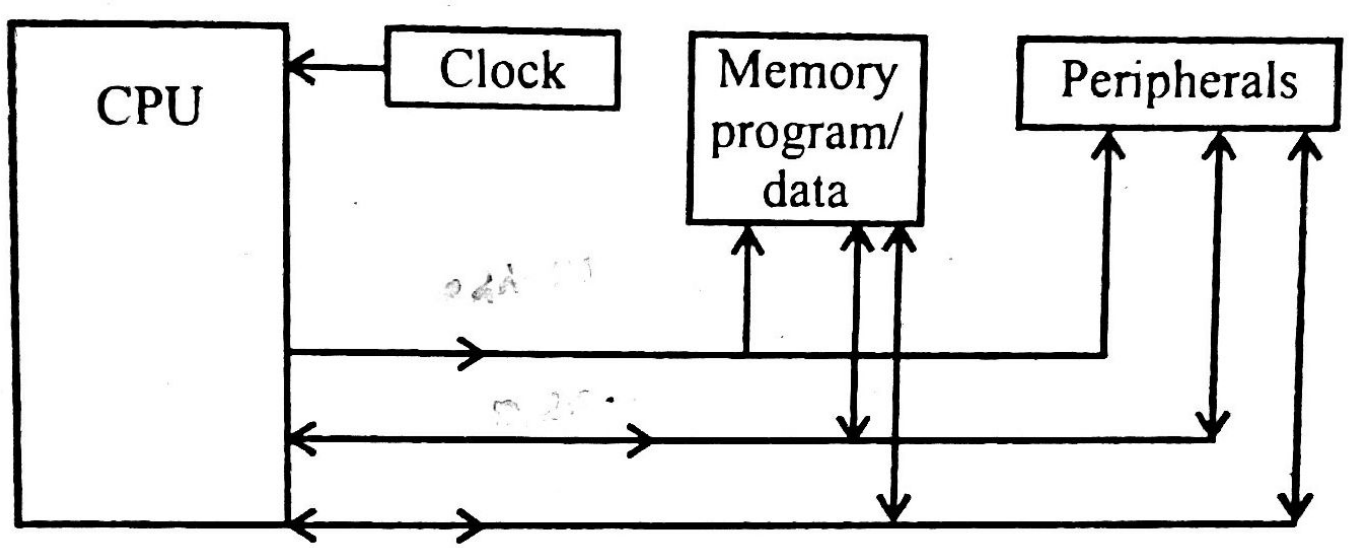
DSP processor to sustain a throughput of one FIR filter tap per instruction cycle, it must perform the following tasks within one instruction cycle.

- Fetch the MAC instruction.
- Read the appropriate sample value from the delay line.
- Read the appropriate coefficient value.
- Write the sample value to the next location in the delay line, in order to shift data through the delay line.

3.3 Architecture of TMS320C64xx processor

Von Neumann Architecture:

- In 1946, John Von Neumann developed the first computer architecture that allowed the computer to be programmed by codes residing in memory.
- Program Instructions were stored in Read Only Memory (ROM).



3.3 Architecture of TMS320C64xx processor

Von Neumann Architecture:

Data Bus:

- Transports data between CPU and its peripherals.
- It is bidirectional. The CPU can read or write data in peripherals.

Address Bus:

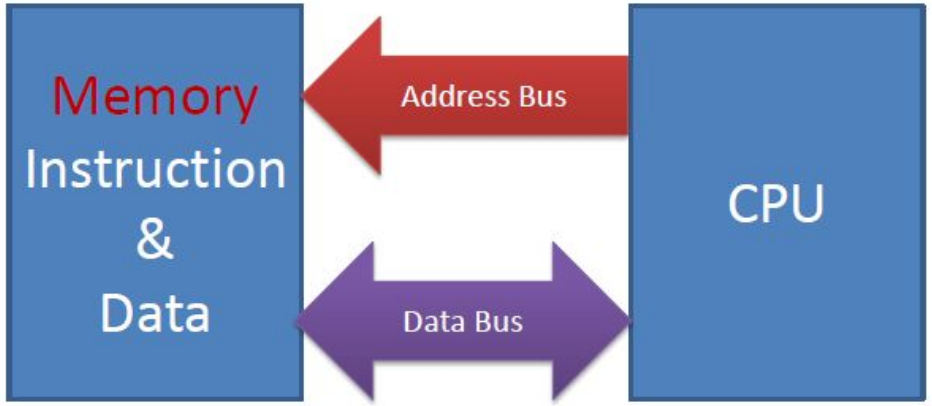
- The CPU uses the address bus to indicate which peripherals it wants to access and within each peripheral which specific register.
- The address bus is unidirectional. The CPU always writes the address, which it read by the peripherals.

3.3 Architecture of TMS320C64xx processor

Von Neumann Architecture:

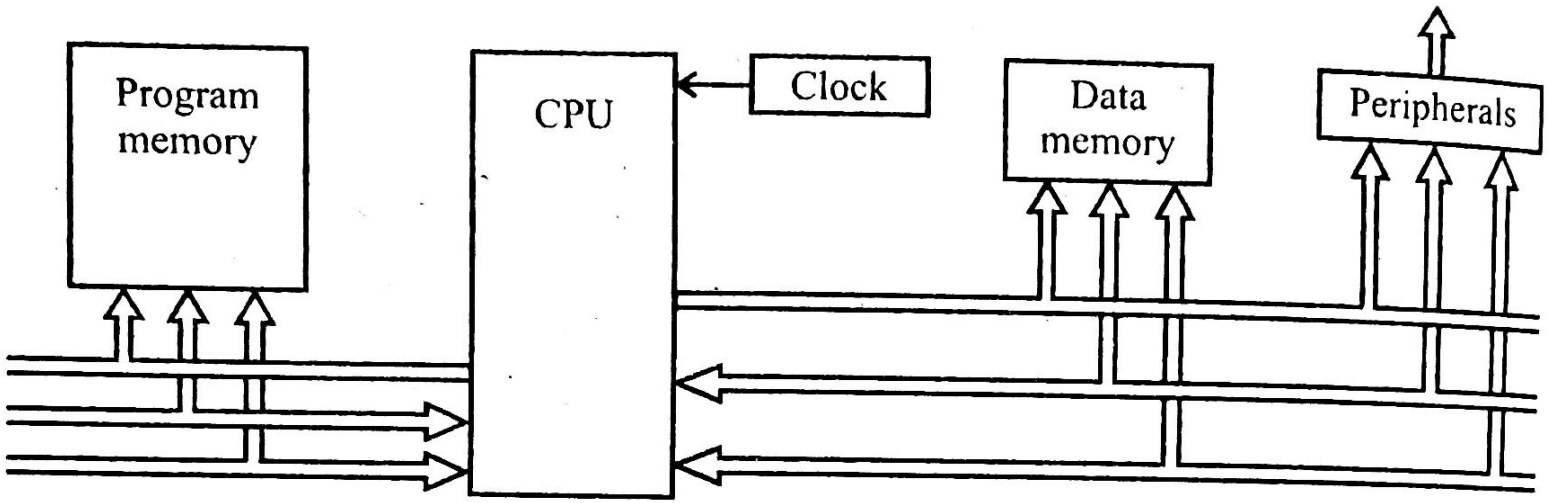
Control Bus:

- The bus carrier signals that are used to manage and synchronize the exchanges between the CPU and its peripherals, as well as that indicates if the CPU wants to read or write the peripheral.



3.3 Architecture of TMS320C64xx processor

Harvard Architecture:



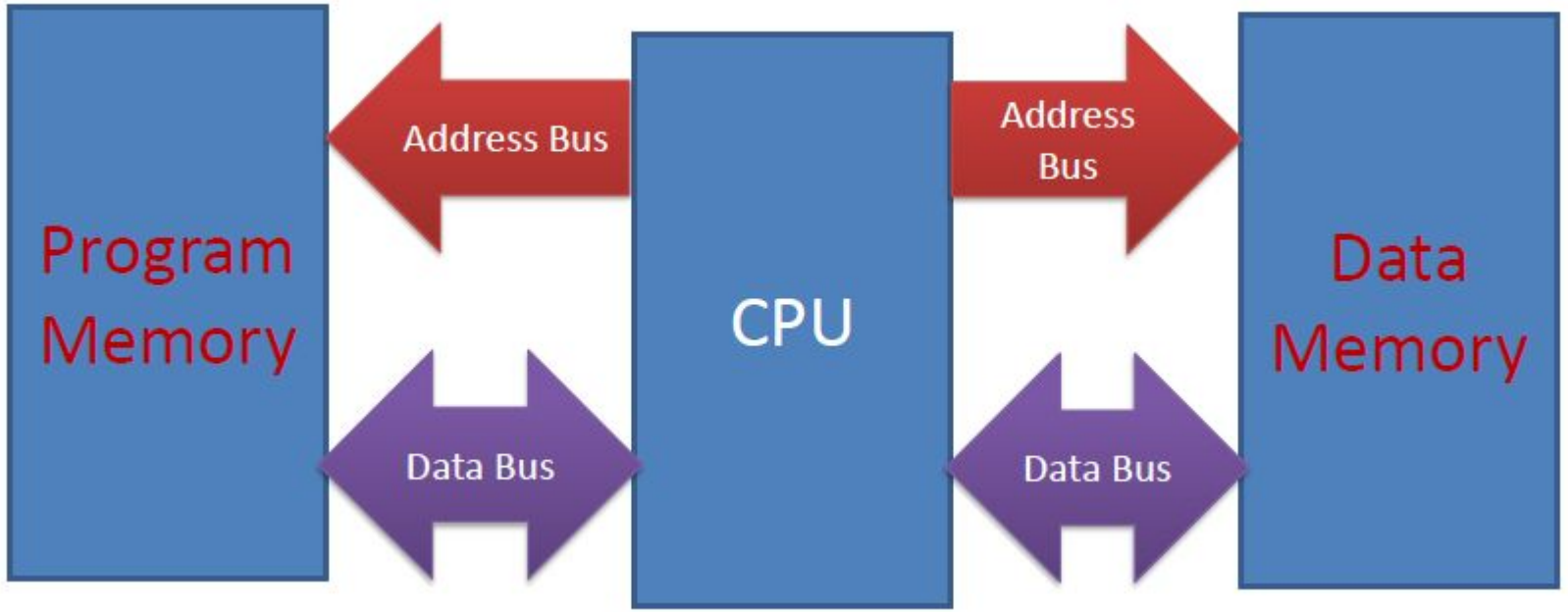
- Harvard architecture is capable of simultaneous reading an instruction code and reading or writing a memory or peripheral as part of the execution of the previous instruction.

3.3 Architecture of TMS320C64xx processor

Harvard Architecture:

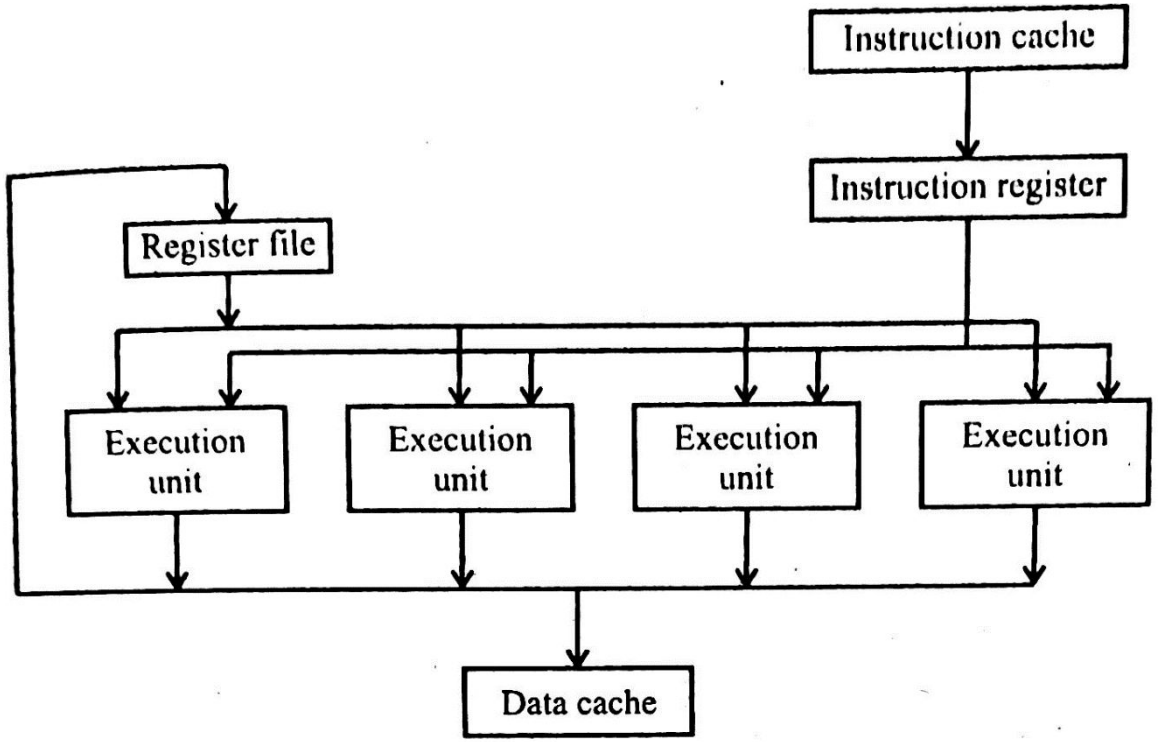
- Since it has two memories, it is not possible for the CPU to mistakenly write codes into the program memory and therefore compute the code while it is executing.
- However it is less flexible. It needs two independent memory banks.
- These two resources are not interchangeable.

3.3 Architecture of TMS320C64xx processor



3.3 Architecture of TMS320C64xx processor

VLIW Architecture



3.3 Architecture of TMS320C64xx processor

VLIW Architecture

- The new architecture that has attracted a great deal of attention in the DSP community is the Very Long Instruction Word(VLIW).
- The very long instruction word processing increase the number of instructions that are processed per cycle.
- It is essentially a concatenation of several short instructions and require multiple execution units, running in parallel, to carry out the instructions in a single cycle.
- VLIW architecture executes multiple instructions/cycle and use simple, regular instruction sets.

3.3 Architecture of TMS320C64xx processor

Advantages of VLIW Architecture

1. Increased performance
2. Better compiler targets
3. Potentially easier to program
4. Potentially scalable
5. Can add more execution units, allow more instructions to be packed into the VLIW instruction.

3.3 Architecture of TMS320C64xx processor

Disadvantages of VLIW Architecture

1. New Kind of programmer/ compiler complexity
2. Program must keep track of instruction scheduling
3. Increased memory use
4. High power consumption
5. Misleading MIPS ratings