Numerical problems:

(Pipelined Processor and Performance measures)

Q1. Consider a processor with a clock rate of 2 GHZ. A program consisting of 200000 instruction is executed on this processor in 2 different setups:

A) Single-core setup: The program takes 0.2 seconds to execute

B) Multi-core setup: The program is executed on a 4-core processor in parallel, Taking 0.8 seconds to complete.

I. Calculate the Clock Per Instruction(CPI) of the program in the single core setup
II. Calculate the the Instruction Per Cycle (IPC) of the single-core setup
III. Determine the execution time for the program in the single-core setup using the CPI Value
IV. Calculate the speedUp achieve by using the multi-core setup compared to the single-core setup.
V. Determine the efficiency of the multi-core setup

Q2. A program consists of three types of instructions: A, B, and C. The execution of these instructions on two processors, P1 and P2, is given below:

Instruction Type	Percentage of Total Instructions	CPI on P1	CPI on P2
A	30%	2	3
B	50%	4	2
C	20%	3	4

Both processors have a clock rate of 2 GHz. The program contains 1 million instructions.

(i) Calculate the total number of clock cycles required to execute the program on P1 and P2.

(ii) Determine the execution time for both P1 and P2.

(iii) Which processor is faster, and what is the speedup of the faster processor compared to the other?

Q3. Consider a 3-stage pipelined processor having a delay
of 10 ns (nanoseconds), 20 ns, and 14 ns, for the first, second, and the third stages,

respectively. Assume that there is no other delay and the processor does not suffer from any pipeline hazards. Also assume that one instruction is fetched every cycle.

The total execution time for executing 100 instructions on this processor is _____ (Gate CSE 2023)

Q4. There is a 5 stage processor having the stages Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO).

If the phases IF, ID, OF, and WO stages take 1 clock cycle. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Operand forwarding is used in the pipeline (for data dependency, OF stage of the dependent instruction can be executed only.

Instruction	Meaning of instruction
I0 : MUL R2 ,R0 ,R1	R2 ¬ R0 *R1
I1 : DIV R5 ,R3 ,R4	R5 ¬ R3/R4
I2 : ADD R2 ,R5 ,R2	R2 ¬ R5+R2
I3 : SUB R5 ,R2 ,R6	R5 ¬ R2-R6

i. Draw the pipeline diagram to show the execution of these instructions.
ii. Calculate the total number of clock cycles required to complete the execution of all instructions assuming no stalls or hazards, and operand forwarding is used.

Q5. Consider a 5-stage instruction pipeline (Fetch, Decode, Execute, Memory, and Write) in a processor. The processor has a clock cycle time of 2 nanoseconds. Assume that there are no pipeline hazards or stalls, and we are executing 20 instructions.

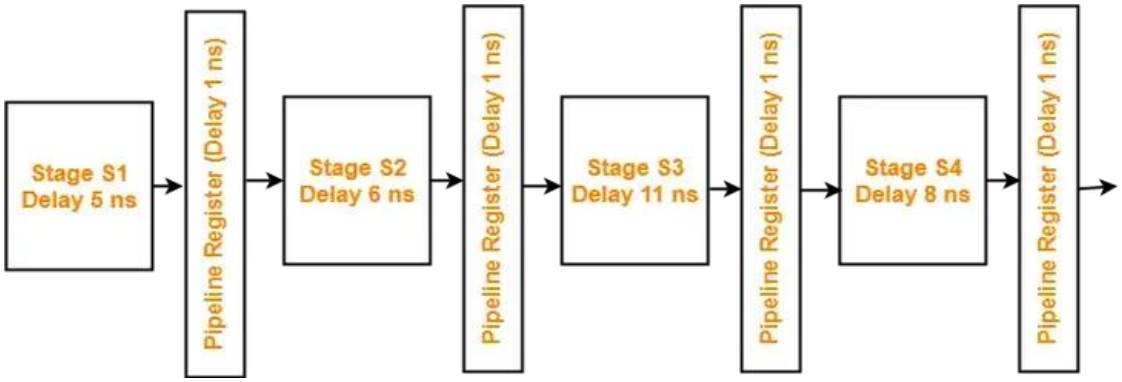
1. Calculate the total execution time of 20 instructions in:

(i) A non-pipelined processor (ii) A pipelined processor

2.If there is a structural hazard that causes a 2-cycle stall for every instruction, how many clock cycles will it take to complete the 20 instructions in the pipeline?

3. Find the speedup achieved by using the pipelined processor (ignoring stalls).

Q6. Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure-



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

Q7. Consider the following procedures. Assume that the pipeline registers have zero latency.

P1 : 4 stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns

P2 : 4 stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns

P3 : 5 stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns

P4 : 5 stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns

Which procedure has the highest peak clock frequency?